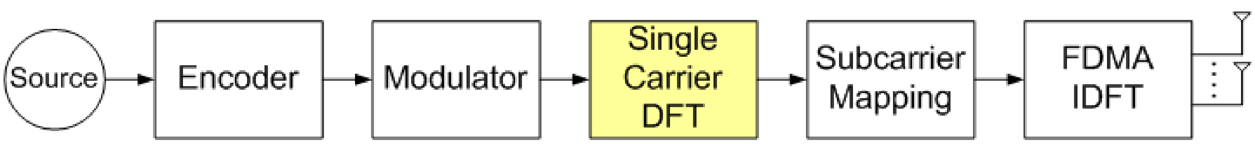
Datasheet: Non-Power-of-Two DFT

Features

- ***Sample Rates**:* Very high clock speeds, e.g., as high as 450MHz in 65nm FPGA technology (highest commercially available FPGA-based throughputs)
- ***FFT size***: any size set of transforms (chosen at run-time) factorable into bases $N=a^n b^m c^r \ldots$, where n,m,r are integers and the bases $a,b,c,\ldots$ are less than ~10. (Examples in this datasheet include the 35 transforms sizes required by LTE SC-FDMA)
- ***Dynamic Range***: combined block floating point and floating point architecture means smaller word lengths can be used for post-processing operations such as equalization (~6db/bit)
- ***Scalability***: array based architecture means arbitrarily higher throughputs are obtained by increasing array size
- ***Power***: array interconnects are entirely local, reducing parasitic routing capacitance to keep power dissipation low and clock speed high
- ***Implementation FPGA***: Centar's DFT circuit can be used in any FPGA fabric containing embedded multipliers and memories
- ***Interface***: simple

Example Usage

LTE Single Channel Frequency Division Multiple Access (LTE SC-FDMA):



LTE Uplink

Options

- Fixed point word input lengths (2's complement)
- Output format
    - Fixed-point
    - Block floating-point
    - Floating-point

Algorithm

The transform computation is based on a new matrix formulation of the discreet Fourier transform[1] (DFT) which decomposes it into structured sets of *b*-point DFTs. This avoids the inherent irregularities of the usual signal flow graph approach which typically requires complex commutators or permutation circuits, variable memory blocks, large butterfly units, global

[1] J. Greg Nash, "Computationally Efficient Systolic Array for Computing the Discreet Fourier Transform, IEEE Trans. Signal Processing, Vol. 53, No.12, December 2005, pp.4640-4641.

interconnections, and stage-to-stage differences, all of which degrade performance and require extra logic resources. Centar's approach uses a small, regular, locally connected array, that keeps interconnect delays lower than cell delays, leading to high clock speeds/throughput and minimizes power. Because the circuit has a "memory based" architecture[2], it is programmable so that a range of transform can be performed on the same array given adequate memory resources. (Data provided here applies to LTE SC-FDMA DFT transform size requirements). Finally, it includes a low overhead hybrid floating-point feature that increases dynamic range for a given fixed-point word size.

Architecture

The architecture consists of a linear array of *b* pipelined, fine-grained, locally connected, simple processing elements, each containing a multiplier, a complex adder, a few registers and multiplexors. By cycling data through this array in a programmable way any size or number of transform sizes can be supported as well as desired variations from the standard DFT calculation. The actual size choices for transforms can be made at run-time. The value of *b* must be equal to or greater than the largest factor in the decomposition of the transform size *N*. For example, if $N=2^n3^m5^r$ then *b* must equal at least 5.

Signal-to-Quantization-Noise-Ratio (SQNR)

Unlike traditional pipelined FFTs, all additions are performed at full precision so that the round-off errors occur only in the twiddle multiplication steps. Consequently, the SQNR is much higher than found in other FFT architectures for a given input bit length.

	SC-FDMA Transform Sizes (12-bit input)				
	36	72	576	864	1296
Mean	68	64	64	64	64
Std. Dev.	1.8	2.9	1.8	1.7	1.7
Maximum	71	74	68	70	67
Minimum	41	42	57	56	56

SQNR (db) (500 FFT blocks)

Performance and Resources

Here Centar's LTE SC-FDMA circuit is compared to commercial designs also implemented in FPGA technologies. In order to provide a more relevant metric than throughput and latency numbers the length of time necessary to compute an LTE resource block (RB), as shown diagrammatically in Fig.5, was chosen. The RB is the minimum processing unit of data for the LTE protocol and occupies one time "slot" (0.5ms), divided up into 7 symbols for (normal cyclic prefix). For example, 1296 subcarriers would imply processing a maximum of 108 RBs. This is a better performance comparison metric in that it requires both low latency and high throughput for good results.

[2] J. Greg Nash, "High-Throughput Programmable Systolic Array FFT Architecture and FPGA Implementations", Presented at the 2014 International Conference on Computing, Networking and Communications (ICNC), Honolulu, HI, Feb 2014.

Xilinx

A Vertix-6 (XC6VLX75T-3) FPGA was used as the target hardware for both the Xilinx and Centar's circuit. The same software tools (ISE 14.7) for synthesis and place-and-route were also used. The Xilinx LogiCORE IP version 3.1 was used to generate a 16-bit version of their DFT because the SQNR of 60.0 db (average over all 35 transform sizes) was comparable to Centar's 12-bit circuit with average SQNR=61.3. (Xilinx LogiCORE includes a bit accurate C model, callable as a Matlab mex function, that was used to obtain Xilinx SQNR values.)

The resource comparisons in the table below use a block RAM normalized to 18K bits, so that a 36K block RAM is considered equal to two 18K RAMs. Also, the "RB Average Throughput" column provides the average number of cycles (over all 35 DFT sizes) it takes to compute the DFT for the 7 symbols defined by a RB as a function of the transform size *N*. Finally, the Fmax (maximum clock frequency) value and the number of RB clock cycles are combined, providing a measure of the throughput, which is normalized to a value of "1" for the Centar design (a higher number is better). So the table shows the Xilinx circuit uses 66% more registers and 32% LUTs, while Centar circuits provides 41% higher throughput. So the overall combined gain is significant.

The Centar design uses more embedded memory and multipliers, but this was less a consideration as discussed in Section I. Also, since many wireless applications involve use of MIMO and cell towers can have three different sectors operating simultaneously, it is possible that more than one single carrier DFT cores could be required. In theory Centar's 41% higher throughputs translate to fewer cores, which reduces considerably the Xilinx advantage in block RAM usage shown in the table.

Intel

Intel does not offer a DFT LTE core as does Xilinx; however, they have published results of an example design running on a Stratix III FPGA with 9K memory blocks that provides a useful basis for comparison.

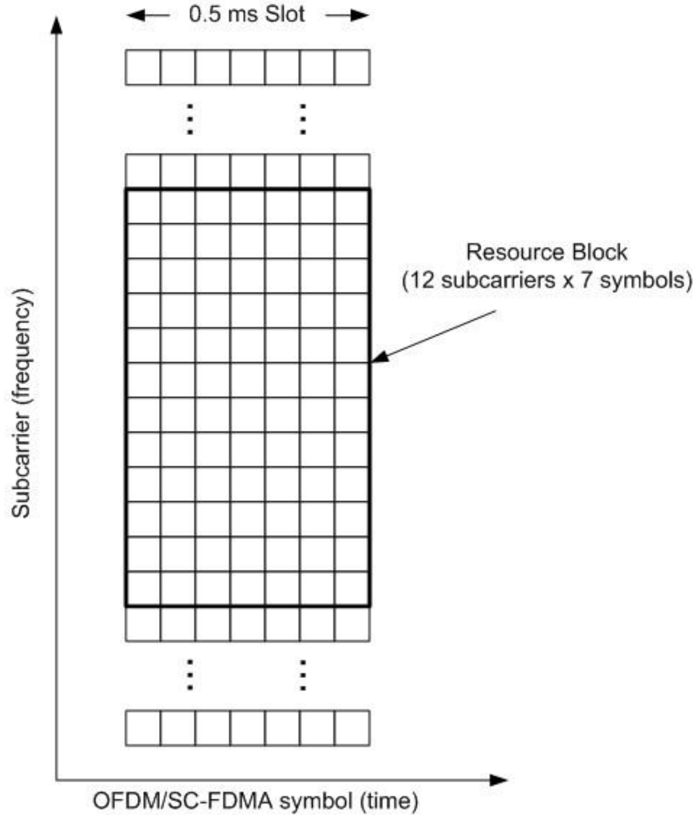


Fig. 5. LTE Resource block definition

For comparison the Centar design was also targeted to a Stratix III FPGA (EP3SE110F780C2) and the same Intel Quartus tools for synthesis and place-and-route were used to implement the design. The Intel implementation uses less logic, but is far slower, both in terms of the lower values of Fmax, and the increased number of cycles to complete the RB computation. Consequently, the Centar design has a significant ~3x higher throughput while LUT usage is only ~47% higher.

Note as well the Intel core doesn't offer a 1296-point transform option and the outputs are not in normal order. Adding buffer circuitry to sort the output data would require additional logic and add ~N additional words of memory (~5 9K RAM blocks) to the numbers shown in the table.

Design	**FPGA**	**LUT**	**Registers**	**Block RAM (9/18K)**	**Multipliers (18-bit)**	**Fmax (MHz)**	**RB Average Throughput (cycles)**	**Throughput (Normalized)**
Centar	Virtex-6	2915	2581	19	72	401	16.6N	1
Xilinx [1]	Virtex-6	3849	4326	10	16	403	23.4N	0.72

Centar	Stratix III	3816	3188	29	60	417	16.6*N*	1
Intel [2]	Stratix III	2600	N/A.	17	32	260	32.9*N*	0.33

To support several sectors with MIMO several Intel cores would need to be used. In this case only one or two Centar cores would be required, so that the Intel block RAM advantage would be nullified, as shown in the table below. Here, the ratios are shown for each of the elements, normalized to the design with the small resource requirement for a particular element. As can be seen, except for the case of having just one sector and no more than two MIMO streams, the Centar design uses significantly fewer LUTs and block RAMs, and slightly fewer multipliers.

Number MIMO Streams	Sectors	Total RB	Intel Cores Required	Centar Cores Required	LUT Intel::Centar	Block RAM Intel::Centar	Multipliers Intel::Centar
1	1	1	1	1	1.00::1.47	1.00::1.32	1.00::1.875
2	1	2	1	1	1.00::1.47	1.00::1.32	1.00::1.875
4	1	4	2	1	1.36::1.00	1.52::1.00	1.07::1.00
1	3	3	2	1	1.36::1.00	1.52::1.00	1.07::1.00
2	3	6	3	1	2.04::1.00	2.27:1.00	1.60::1.00
4	3	12	4	2	1.36::1.00	1.52::1.00	1.07::1.00

Operation as high as 450MHz has been verified using an Intel Stratix III development kit, which included an EP3SL150F1152C2 FPGA.

Device Family Support

Intel Device Families Supported

- Stratix
- Aria
- Cyclone
- Hardcopy

Xilinx Device Families Supported

- Virtex 4-7
- Spartan
- Artix-7

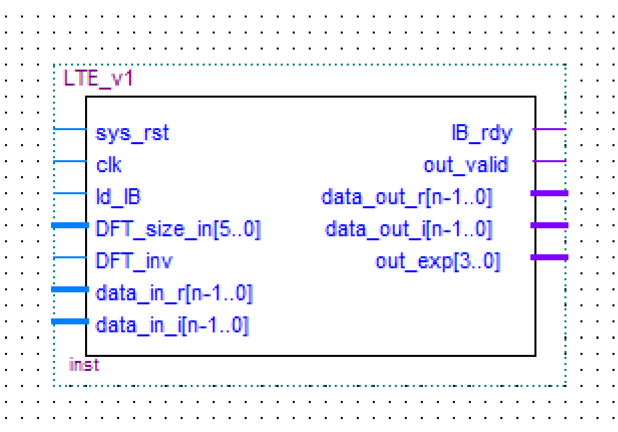
Deliverables

- Netlist (e.g., for Intel FPGAs a verilog *.qxp file for synthesis or *.vo file for simulation)
- Synthesis constraints (e.g., for Intel FPGA's an *.sdc file)

- Modelsim LTE SC-FDMA Testbench (*.vo file for DFT circuit plus verilog testbench control file) that reads data from input file and outputs transform data to output file. Also includes Matlab verification utilities
- Quartus LTE SC-FDMA Test benches (35 DFT sizes, 12-points to 1296-points) that include pin-outs for use with an Intel Stratix III FPGA board development kit
    1. On-chip input/output data memories and a *.qxp file for the DFT circuit, that performs user selected number of blocks for a single size DFT
    2. On-chip input/output data memories, verilog control circuitry, and a *.qxp file for the DFT circuit that cycles continuously through 2 blocks each of the LTE 35 different DFT sizes
    3. Modelsim simulation environment of (2) using *.vo file.
- Matlab behavioral bit-accurate model (p-code) for LTE SC-FDMA DFT sizes
- Documentation for above

Pin-outs

A symbol list corresponding to the pin-outs shown below are provided in the accompanying table. These apply to the "nominal variable" FFT circuit. For example some of the test benches do not include data I/O. Depending upon the desired interfaces, other signals could change.



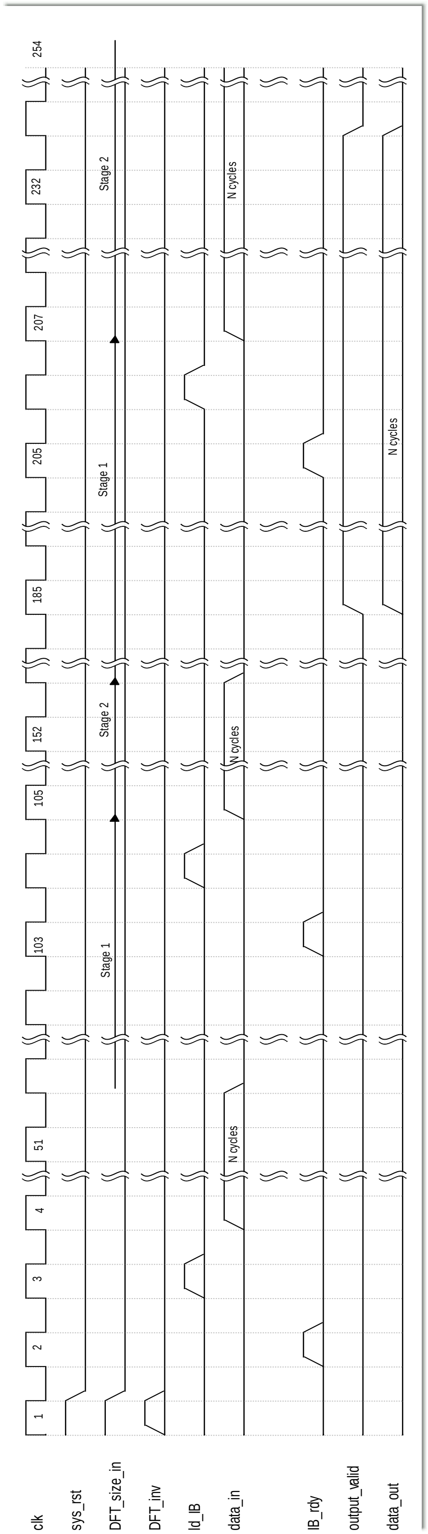
Name	Signal	Description
clk_IO_in	clock	Can be either a low frequency board oscillator clock output in which case circuit clock is derived from a PLL or actual data I/O clock
sys_rst	control	Resets circuit; active high
DFT_size_in	control; 5-bits unsigned	Registers DFT size
DFT_inv	control	Low->forward; high->inverse
data_in_r/i	n-bit signed	Real and imaginary inputs; signed fixed-point
IB_rdy	control	Input buffer ready for data
out_valid	control	

out_exp	4-bits unsigned data	Exponents (one per real/imag data pair)
data_out_r/i	n-bit signed data	Real and imaginary mantissa outputs

Timing Diagram

A variety of timing possibilities exist depending upon the desired interface. That shown here is applicable to an example 48-point DFT, but other sizes will have the same form.

When *sys_rst* goes high, the size and direction of the transform are latched. After the circuit generates *IB_rdy*, the external data source generates *ld_IB*, and on the next clock cycle the circuit expects to see *N* data values on the next *N* cycles. Valid data out occurs when *output_valid* goes high:


clk
sys_rst
DFT_size_in
DFT_inv
ld_IB
data_in
IB_rdy
output_valid
data_out
1
2
3
4
51
103
105
152
185
205
207
232
254
Stage 1
Stage 2
Stage 1
Stage 2
N cycles
N cycles
N cycles
N cycles

For small DFTs, e.g., 12/24/36 points in the LTE protocol, streaming I/O is performed (continuous input and output) and the timing diagram is (for 12 points):